REMARKS

Status of Claims

Claims 1-9, 12, 16, 21-22, and 39-52 were pending at the time of Examination of the Final Office Action dated March 19, 2004.

In the Amendment filed on June 16, 2004, Applicant canceled pending Claims 1-9, 12, 16, 48-49 in the listing of the Claims. Accordingly, after entry of the Amendment, Claims 21-22, 39-47, 50-52 were pending in the Application.

The Examiner commented in the Advisory Action dated July 1, 2004 that "It is unclear to which claims are canceled. 1-20 or 1-9, 16, 48 and 49." To the extent there was inconsistency between: (1) the instruction "Please cancel claims 1-9, 16, 48 and 49." at the top of Page 2 of the Amendment which would have resulted in Claim 12 being pending instead of canceled; and (2) the listing of the claims at pages 2-7 of the Amendment indicating that Claims 1-20 are canceled thus canceling Claim 12, Applicants hereby assert that Claim 12 was canceled in the listing of the claims. Applicants note that Claims 48-49 were canceled in both the instruction and the listing of the claims.

Thus, as set forth above, after entry of the Amendment, Claims 21-22, 39-47, 50-52 were pending in the Application. Applicants note that the PAIR system at the USPTO website indicates that the Amendment filed on June 16, 2004 was entered. Accordingly, the listing of claims in this Supplemental Amendment are relative to the listing of claims in the Amendment filed on June 16, 2004, which has been entered.

In this Supplemental Amendment, new Claims 53-65 have been added. Claims 53-65 reinstate and renumber canceled Claims 1-9, 12, 16, and 48-49, respectively. Accordingly, Claims 21-22, 39-47, 50-65 are pending in the application after entry of this Supplemental Amendment. Applicants respectfully submit that the claims read upon the species elected in the Amendment letter filed on October 24, 2002.

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Request for Applicant Initiated Examiner Interview.

Co-filed herewith is an Applicant Initiated Interview Request Form, PTOL-413A requesting an interview with the Examiner prior to issuance of the next communication from the USPTO.

Response to the Final Office Action of March 19, 2004.

With regards to Claims 21-22, 39-47, 50-52, the rejections are fully addressed in the Amendment filed on June 16, 2004, which has been entered and is herein incorporated by reference in its entirety. For the convenience of the Examiner, the arguments set forth in the Amendment filed on June 16, 2004 with respect to Claims 21-22, 39-47, 50-52 are represented herein.

Further, the rejection of canceled Claims 1-9, 12, 16, and 48-49 shall be discussed as applied to new Claims 53-65, respectively.

The Drawings satisfy 37 CFR 1.83(a).

The Examiner states:

> The drawings must show every feature of the invention specified in the claims. Therefore, the **insulator coupled to and covering the entire first surface of the second semiconductor chip** and having opposed first and second surfaces; and an insulator coupled to and covering the entire first surface of the second semiconductor chip, **wherein the insulator is coupled between the adhesive layer and the first surface of the second semiconductor chip** in claim 1, must be shown or the feature(s) canceled from the claim(s). (Final Office Action, page 2, emphasis in original.)

Applicants respectfully submit that the features of Claim 53 (corresponding to canceled Claim 1) are shown in the drawings. For example, with reference to FIG. 1, Applicants' specification sets forth:

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> An **insulator 4** is formed on **the first surface 2a of the second semiconductor chip 2**. That is, the insulator 4 formed on the first surface 2a of the second semiconductor chip 2 **is bonded on the upper part of the adhesive layer 3**. (Page 6, lines 6-9, emphasis added.)

Accordingly, the features of Claim 53 are shown at least in FIG. 1 and thus the drawings satisfy 37 CFR 1.83(a).

For the above reasons, Applicants request reconsideration and withdrawal of the objection to the drawings.

Claims 53-61, 62, 63, (corresponding to canceled Claims 1-9, 12, 16, respectively), 21-22, 39-47, 64-65 (corresponding to canceled Claims 48-49, respectively) satisfy 35 U.S.C. § 112, second paragraph.

With regards to Claims 21-22 and 39-47, as set forth in the Amendment filed on June 16, 2004:

Regarding claim 21, below is an annotated version of claim 21, wherein reference numbers from the exemplary embodiment of Figure 1 are inserted into the claim.

21. (Previously Amended) A semiconductor package (11) comprising:

a first semiconductor chip (1) having opposed first (1a) and second (1b) surfaces, the second surface including a plurality of pads (1c);

an adhesive layer (3) coupled to the second surface (1b) of the first semiconductor chip (1); and

a second semiconductor chip (2) stacked over the second surface (1b) of the first semiconductor chip (1) and having opposed first (2a) and second (2b) surfaces; and

an insulator (4) coupled to the first surface (2a) of the second semiconductor chip (2),

wherein the insulator (4) is coupled between the first surface (2a) of the second semiconductor chip (2) and the adhesive layer (3), and is between the first surface (2a) of the second semiconductor chip (2) and each of the pads (1c) of the second surface (1b) of the first semiconductor chip (1).

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Claim 21's recitation of an insulator "between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip" clearly is shown in the example of Figure 1. In particular, the exemplary insulator 4 is overlying the bond pads 1c, and hence is "between" the bond pads 1c and the lower surface 2a of the upper semiconductor chip 2. Accordingly, the rejection of claim 21 under 35 U.S.C. 112 should be withdrawn, because the claim is completely understandable in view of Figure 1. Note that the placement of the insulator 4 over the bond pads 1c enables the feature that "the first conductive wires 5 do not directly contact to the first surface 2a of the second semiconductor chip 2." (Page 7, line 22 et seq.)

Regarding claim 39, below is an annotated version of claim 39, wherein reference numbers from the exemplary embodiment of Figure 1 are inserted into the claim.

39. (Previously Amended) A semiconductor package (11) comprising:
a substrate (7);
a first semiconductor chip (1) coupled to the substrate (7), the first semiconductor chip (1) having opposed first (1a) and second (1b) surfaces;
a second semiconductor chip (2) having opposed first (2a) and second (2b) surfaces;
a first means (3) coupled to the second surface (1b) of the first semiconductor chip (1) for coupling the first semiconductor chip (1) to the second semiconductor chip (2) in a stack;
at least one pad (1c) formed on the second surface (1b) of the first semiconductor chip (1); and
at least one first conductive wire (5) connecting the at least one pad (1c) of the first semiconductor chip (1) and the substrate(7);
at least one pad (2c) formed on the second surface (2b) of the second semiconductor chip (2);
at least one second conductive wire (6) connecting the at least one pad (2C) of the second semiconductor chip (2)and the substrate (7); and
an insulator (4) coupled between the first surface (2a) of the second semiconductor chip (2) and

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the first means (3), and overlying both the first means (3) and the at least one first conductive wire (5).

Claim 39's recitation of "an insulator coupled between the first surface of the second semiconductor chip and the first means, and overlying both the first means and the at least one first conductive wire" clearly is shown in Figure 1. The exemplary insulator 4 is coupled between the adhesive layer 3 and first surface 2a of the second semiconductor chip, and also is directly over both the adhesive layer 3 and the first conductive wires 5. In fact, in the example of Fig. 1, the conductive wires 5 contact the overlying portions of insulator 4, as is shown clearly in Figs. 1A and 1B. Accordingly, the rejection of claim 39 under 35 U.S.C. 112 should be withdrawn, because the claim is completely understandable in view of the figures.

Accordingly, it is submitted that no amendments to the drawings are necessary, and that claims 21 and 39 are allowable with respect to 35 U.S.C. 112, second paragraph.

Further, Applicants respectfully submit that Claim 53 (corresponding to canceled Claim 1) satisfies 35 U.S.C. 112, second paragraph for reasons similar to Claims 21 and 39.

Further, as noted above, Applicants' specification sets forth:

> An **insulator 4** is formed on **the first surface 2a of the second semiconductor chip 2**. That is, the insulator 4 formed on the first surface 2a of the second semiconductor chip 2 **is bonded on the upper part of the adhesive layer 3**. (Page 6, lines 6-9, emphasis added.)

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Applicants respectfully submit that one of skill in the art would understand what is being claimed in Claims 21, 39 and 53 when read in light of the specification. Accordingly, Claims 21, 39 and 53 satisfy 35 U.S.C. 112, second paragraph. Claim 22, which depends from Claim 21, satisfies 35 U.S.C. 112, second paragraph, for at least the same reasons as Claim 21. Claims 40-47, which depend from Claim 39, satisfy 35 U.S.C. 112, second paragraph, for at least the same reasons as Claim 39. Claims 54-65, which depend from Claim 53, satisfy 35 U.S.C. 112, second paragraph, for at least the same reasons as Claim 53.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 50-52 are novel over Pai et al.

As set forth in the Amendment filed on June 16, 2004:

Claims 50-52 were rejected under 35 U.S.C. 102(e) as anticipated by Pai et al. The rejections are respectfully traversed.

Regarding claim 50, Pai et al. lack claim 50's feature of "an insulator coupled to the first surface of the second semiconductor chip, said insulator *being between each of the conductive wires and the first surface of the second semiconductor chip.*" Pai et al.'s film adhesive layer 166 is coupled to the lower surface of the upper semiconductor chip 130, but is entirely inward of the bonding wires 150 that are coupled to the lower semiconductor chip 110. Accordingly, because Pai et al. lack an insulator "between each of the bond wires and the first surface of the second semiconductor chip," the rejection of claim 50 must be withdrawn.

Regarding claim 51, Pai et al. lack claim 51's feature of "an insulator coupled to the first surface of

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the second semiconductor chip, said insulator *being between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip.*" Pai et al.'s film adhesive layer 166 is coupled to the lower surface of the upper semiconductor chip 130, but is entirely inward of the bond pads of the lower semiconductor chip 110. Accordingly, since Pai et al. lack the feature of an insulator "between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip, the rejection of claim 51 must be withdrawn.

Claims 53-55, 57, 59-61, 62, (corresponding to canceled Claims 1-3, 5, 7-9, 12), 21-22, 39-47, 64-65 (corresponding to canceled Claims 48-49) are patentable over Pai et al.

With respect to Claims 21-22 and 39-47, as set forth in the Amendment filed on June 16, 2004:

It is respectfully submitted that claims 21 and 39 distinguish Pai et al., and hence the rejection of those claims and their respective dependent claims is respectfully traversed.

In particular, claim 21's feature of "an insulator" coupled "between the first surface of the between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip" is not shown in U.S. Patent 6,503,776 to Pai et al., because Pai et al.'s adhesive layer 162, dummy chip 160, and film adhesive 166 are entirely inward of the bonding pads of the semiconductor chip 110. Pai et al. show nothing in their Fig. 8 between the bonding pads of the semiconductor chip 110 and the lower surface of the upper

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semiconductor chip 130. Accordingly, claim 21 should be allowed.

Claim 39 also distinguishes Pai et al., because Pai et al.'s adhesive layer 162, dummy chip 160, and film adhesive 166 do not overlie the bond wires 150 coupled to the bonding pads of the lower semiconductor chip 110. Accordingly, Pai et al. lack claim 39's feature of "an insulator overlying both the first means and the at least one first conductive wire."

Since claims 21 and 39 distinguish Pai et al., these claims should be allowed, along with their respective dependent claims.

Further, with respect to Claims 53-55, 57, 59-62, 64-65, the rejection is respectfully traversed.

The Examiner states:

> Pai et al. … specifically figure 8 show a semiconductor package comprising: **a first semiconductor chip 110** having opposed first and second surfaces; **an adhesive layer 166** coupled to the second surface of the first semiconductor chip; **a second semiconductor chip 130 or 160** stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; **and an insulator 166** coupled to and covering the entire first surface of the second semiconductor chip, wherein the insulator is coupled between the adhesive layer and the first surface of the second semiconductor chip. (Final Office Action, page 5, emphasis added.)

Accordingly, the Examiner asserts that the film adhesive 166 of Pai et al. is both "an adhesive layer 166" and "an insulator 166". In support of the Examiner's assertion, the Examiner further states:

> Therefore, it would have been obvious to one of ordinary skill in the art to use the adhesive and the insulator as "merely a matter of obvious engineering

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> choice" as set forth in the above case law. (Final Office Action, page 6.)

The Examiner's statement is respectfully traversed. Applicants respectfully submit that the Examiner has failed to provide any support for the conclusion that to use the adhesive and the insulator [is] "merely a matter of obvious engineering choice". Applicants submit that Pai et al. actually teaches away from such a conclusion.

Pai et al. teaches the criticality of providing clearance between the two chips for the loops of the bonding wires so as to **prevent the bonding wires from contacting the chip.** Accordingly, there is no need for an insulator and clearly the use of an insulator is therefore not an obvious engineering choice. Specifically, Pai et al. teaches:

> Therefore, **the semiconductor industry** develops a stacked chip package 200 (see FIG. 2) characterized by using a dummy chip 160 **to provide clearance between the chips for the loop of the underlying bonding wire.** (Col. 1, lines 64-67, emphasis added.)

For at least the above reasons, Pai et al. does not teach or suggest:

> A semiconductor package comprising:
> a first semiconductor chip having opposed first and second surfaces;
> **an adhesive layer coupled to the second surface of the first semiconductor chip;**
> a second semiconductor chip stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces; and
> **an insulator coupled to and covering the entire first surface of the second semiconductor chip**, wherein **the insulator is coupled between the adhesive layer and the first surface of the second semiconductor chip,**

as recited in Claim 53, emphasis added. Thus, Claim 53 is allowable over Pai et al. Claims 54-55, 57, 59-62, 64-65,

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which depend from Claim 53 are allowable for at least the same reasons as Claim 53.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Claims 21-22, 39-47, 50-65 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 16, 2004.

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Date of Signature

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